ANALOG DEVICES

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APPLICATION NOTE

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Simple DAC-Based Circuit Implements Constant Linear Velocity (CLV) Motor Speed Control

by John Wynne

Most hard-disk and floppy-disk magnetic drives operate with the disk spinning at a constant speed and the READ/WRITE head transferring information to or from the disk at a constant rate. This type of recording is called constant angular velocity (CAV) recording since each data-bit call is given the same angular velocity regardless of its position on this disk surface. However, the size of the data bits will vary depending on their location. Closest to the hub the bit-cell density is maximum thinning out to a minimum nearest the disk circumference. This non-uniform areal bit density (number of bits in a given area) is obviously wasteful of disk space.

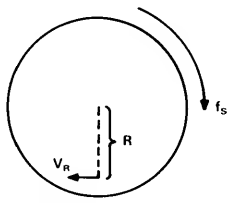
CD-ROM drives—and CD players—employ a different type of recording technique in order to achieve a constant areal bit density over the operating disk surface. These drives use constant linear velocity (CLV) recording, a technique which actually varies the speed of the spinning disk according to where the data-bit cell is located. Disk speed is highest for cell locations closest to the hub with decreasing speed for cell locations towards the disk circumference. Varying the rotational speed ensures that the distance between data-bit cells is constant regardless of cell location, and it also maintains a constant data transfer rate from the disk. CLV recording can boost disk capacity by up to 35% over that achievable with CAV recording. However, one of the drawbacks to this technique is the relatively long access times due to the required speeding-up or slowing-down of the disk.

It is somewhat ironic that the first generation of optical CD-ROM drives on the market in the main ignored the capacity boost possible with CLV (an ideal drive for optical drives because of the continuous spiral track on which data is recorded) and concentrated instead on reducing the seek times in order to compete with high density hard-disk drives. Some manufacturers have introduced drives which go some way towards combining the high density offered by CLV with the fast access times offered by CAV by using a technique called banding or zoning. In this approach the surface of the disk is divided into a small number of concentric bands or zones. Within each band the recording is CAV. From band to band a degree of CLV is achieved, not by changing the rotational speed of the disk, but by changing the data recording rate for each new band. This complicates the design of the controller somewhat since a variable frequency phase-locked loop (PLL) will be required for the data-separator circuit. If access times are the only yardstick by which different drives are to be compared then CAV-recorded disks will inherently be faster than CLV-recorded disks. However many applications exist where disk capacity is as important as, if not greater than, data access times; archival applications being an obvious one. CLV recording with its substantial capacity advantage will be the drive of choice in these areas.

The circuit presented here produces a transfer characteristic which mimics exactly the relationship between data-bit cell position (i.e., head position) and disk rotational speed required to achieve CLV recording. In mimicking this relationship the DAC digital input data represents the radius at which the READ/WRITE head is to be positioned, while the circuit output voltage represents the correct rotational speed for that head position. By employing such a circuit in a servo loop controlling the speed of the spindle motor it should be possible to directly program the correct disk speed for any data location on the disk resulting in faster data access times.

SPEED VS. POSITION

For any rotating system, spindle speed and linear velocity are related by the simple expression (see Figure 1).



$V_R = 2\pi f_S R$

V_R = LINEAR VELOCITY

f_S = SPINDLE SPEED

R = RADIAL POSITION

Figure 1. Pictorial Explanation of Terms

$$V_R = 2\pi f_S R \quad (1)$$

where V_R is the linear velocity

f_S is spindle speed

R is radial position

Essentially V_R is the velocity of the disk passing under the READ head. This linear velocity must remain constant over the operational area of the disk in order to ensure a constant data transfer rate. For this to happen the spindle speed must be inversely proportional to the radial position of the head or

$$f_S = \frac{V_R}{2\pi R} \quad (2)$$

An optical drive platter has maximum and minimum radii between which the data is stored. The radial position of the READ head can be expressed in terms of these limits as

$$R = R_{MIN} + X(R_{MAX} - R_{MIN}) \quad (3)$$

where R_{MIN} is the minimum operating disk radius,

R_{MAX} is the maximum operating disk radius,

X is a fractional representation of the required head position, $0 \leq X \leq 1$.

Substituting this expression into the previous one and normalizing the result to the highest spindle speed produces a ratioed expression as

$$f_{RATIO} = \frac{f_S}{f_{S\,MAX}} = \frac{1}{1+X\left(\frac{R_{MAX}}{R_{MIN}}-1\right)} \quad (4)$$

The READ head at the minimum radius corresponds to X = 0 and has the highest spindle speed. As X increases towards the outer edge of the disk the spindle speed decreases. The shape of this curve is shown in Figure 2.

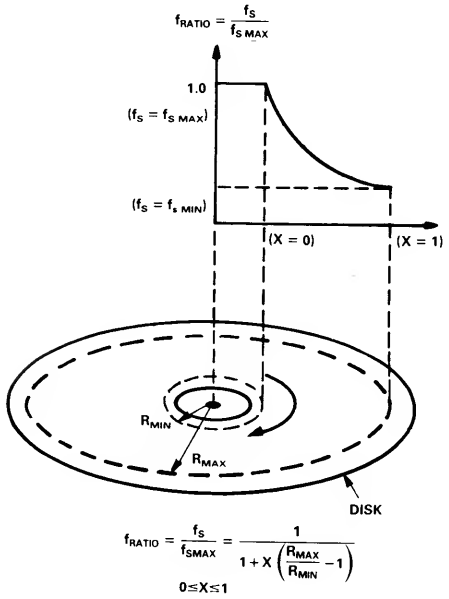


Figure 2. Relationship Between Disk Spin Speed and Head Position for a Constant Linear Velocity

The minimum value of f_{RATIO} depends on the disk diameter. For example, with a disk of diameter 12 inches, R_{MAX} could be 5 inches and R_{MIN} be 2 inches. This means f_{RATIO} varies from 1.0 to 0.4, i.e., the minimum speed is 0.4 f_S max.

THE MIMICKING CIRCUIT

The circuit in Figure 3 has a transfer function equal to

$$V_{RATIO} = \frac{V_{OUT}}{V_{REF}} = \frac{1}{1+D1\frac{R_{FB}}{R_{DAC1}}} \quad (5)$$

where D1 is a fractional representation of the DAC digital input data and can vary from 0 to almost unity and R_{DAC1} is the ladder resistance of DAC 1.

Note that

$$D1 = \frac{N1}{2^n} \quad (6)$$

where N1 is digital input data in decimal and

n is resolution of DAC.

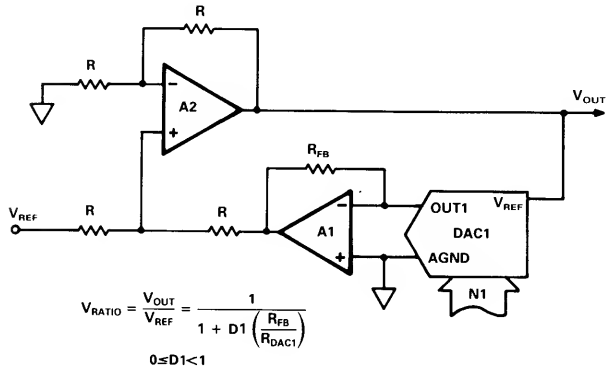


Figure 3. Circuit to Mimic the Speed/Position Curve of Figure 2

The V_{RATIO} transfer function of Expression (5) mimics the required f_{RATIO} relationship of Expression (4) exactly. The value of the R_{FB}/R_{DAC1} ratio in Figure 3 is dependent on the DAC resolution and the R_{MAX}/R_{MIN} ratio which is fixed for a given disk diameter and can be found by equating the denominators of Expressions (4) and (5) as:

$$\frac{R_{FB}}{R_{DAC1}} = \frac{X}{D1}\left(\frac{R_{MAX}}{R_{MIN}}-1\right) \quad (7)$$

Using the R_{MAX} and R_{MIN} values from the previous example and a 12-bit resolution DAC and solving Expression (7) when X = 1 and D1 = 4095/4096 yields an R_{FB}/R_{DAC1} ratio of 1.5004. Due to the manufacturing spread in DAC ladder resistance, implementing the required R_{FB}/R_{DAC1} ratio on a production basis is itself an interesting exercise and will be dealt with separately [see later].

Using The Circuit

A block diagram of a possible motor speed controller incorporating the DAC circuit is shown in Figure 4. The effect of the DAC circuit is to augment the existing motor speed control circuitry (shown in dashed box) by providing a coarse feedback signal which very quickly ensures the disk is speeded up or slowed down to the proper speed after a new SEEK command is received. When the READ head approaches its correct new position, motor control is handed back to the fine-speed control elements within the dashed box.

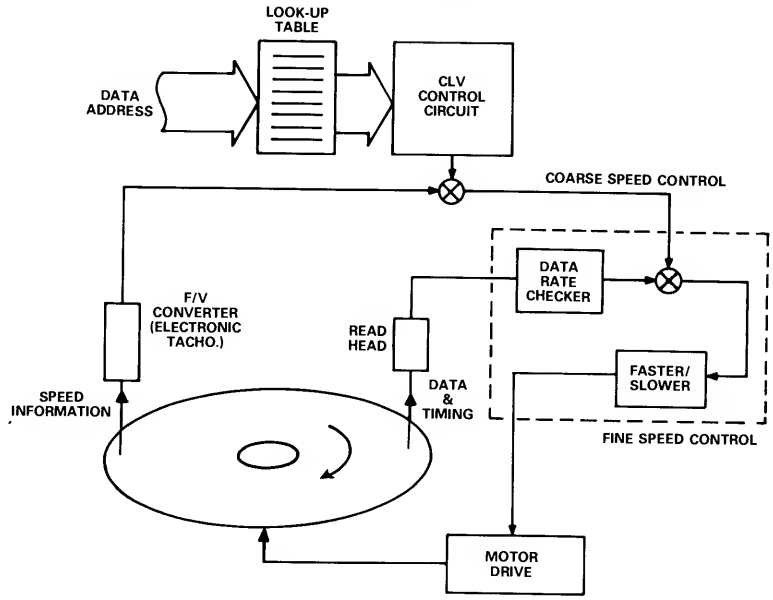


Figure 4. Block Diagram of CLV Motor Speed Controller with Coarse and Fine Speed Control Loops

The disk look-up table in Figure 4 performs the task of changing absolute data addresses into corresponding fractions of the disk radius. Figure 5 shows the "transfer curve" for the digital-in, digital-out look-up table. The curve is nonlinear reflecting the fact that with constant density recording more data locations are available as the spiral track circumference increases, i.e., towards the edge of the disk. With CAV recording this relationship would be linear reflecting the fact that each track across the disk surface has the same amount of data on it.

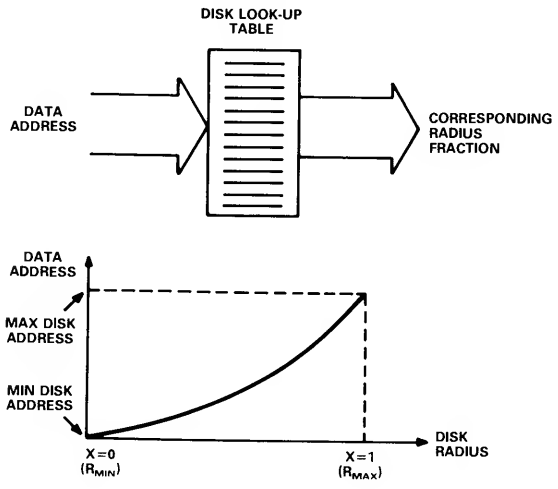


Figure 5. Relationship Between Disk Data Address and Corresponding Location on Disk Surface

The number of look-up values in the table is equal to or less than the resolution of the DAC being used. With a 12-bit DAC such as the AD7545, 4096 different disk speeds are programmable, hence the look-up table need be no bigger than 4096 entries. Each of these different speeds corresponds to a block of contiguous data addresses. The fine speed control circuitry can differentiate (if required) between data addresses and hence disk speed in any one block. Using a higher resolution DAC obviously increases the number of programmable speeds available, e.g., a 14-bit DAC such as the AD7538 allows 16,384 speeds to be programmed. As an example of the system in operation in a CD-ROM drive, consider that the READ head is positioned at the minimum disk radius R_{MIN}. At this radius the disk will be revolving at its maximum speed f_S max, typically 900 rpm. A SEEK command to read data from an address corresponding to a position 3/4 of the way across the operating disk area requires that the disk speed be reduced by 53% to 423 rpm, an f_{RATIO} of 0.47 (from Equation 4 and using an R_{MAX}/R_{MIN} ratio of 2.5). The error signal to achieve this reduction is generated by loading the digital equivalent (or the closest code possible) of the fractional 3/4 distance into the DAC. In this example the most suitable code, N, is 3072_{10} which is loaded from the look-up table. From Equation (5) the output voltage of the circuit will now be 0.47 V_{REF}, a V_{RATIO} of 0.47. The signal is compared with the output of the linear frequency/voltage converter whose output voltage at f_S max is

V_{REF}.. The difference between these two signals is the coarse error signal which drives the disk to its correct speed of 423 rpm. The same code, 3072_{10}, from the look-up table is loaded into another DAC producing a voltage which will drive the head to the required position, 3/4 of the way across the disk surface. Figure 6 shows this coarse head positioning loop with a voice coil motor driving the laser head assembly.

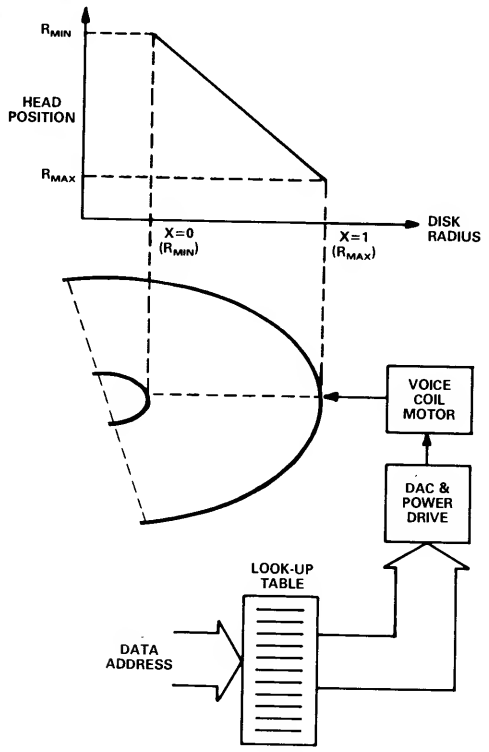


Figure 6. Coarse Control Loop for Positioning Head Assembly

IMPLEMENTING THE R_{FB} /R_{DAC1} RATIO

Standard CMOS DAC manufacturing strives to make the on-chip feedback resistor R_{FB} as equal as possible to the DAC ladder resistance R_{DAC}. The circuit of Figure 3 relies on being able to choose an R_{FB}/R_{DAC1} ratio which is not unity but dictated by the system parameters of disk size and number of programmable speeds required, i.e., DAC resolution. Equation 7 gives the exact relationship between these parameters. Since the required R_{FB}/R_{DAC1} ratio is always going to be greater than unity, the obvious solution is to add a resistor R1 in series with the feedback resistor, Figure 7.

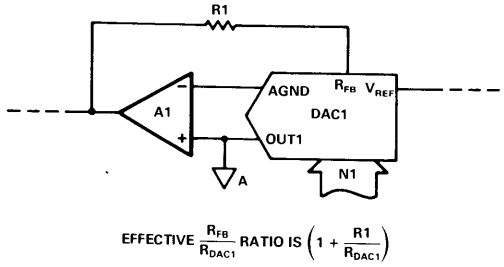


Figure 7. Incorrect Way to Implement R_{FB}/R_{DAC1} Ratio

There are two drawbacks to this solution. The first is that R1 would have to be a select-on-test resistor due to the manufacturing spread in absolute values of the DAC ladder resistance. Typically the spread is ±20% around a mean value of 11kΩ. A second drawback is that for significant changes in gain, R1 will be large relative to the DAC resistors and its temperature coefficient is unlikely to match the temperature coefficient of the DAC, typically −300ppm/°C. As a result such a gain trim would exhibit large temperature coefficients.

One solution to realizing nonstandard, repeatable gain factors uses three additional resistors as shown in Figure 8. Resistors R1, R2 and R3 should all have similar temperature coefficients, but they need not match the temperature coefficient of the DAC. The overall gain depends only on the values of external resistors and excludes the absolute value of the ladder itself. Gain is best adjusted by varying the attenuator ratio, as adjustment sensitivity is almost unaffected by R1.

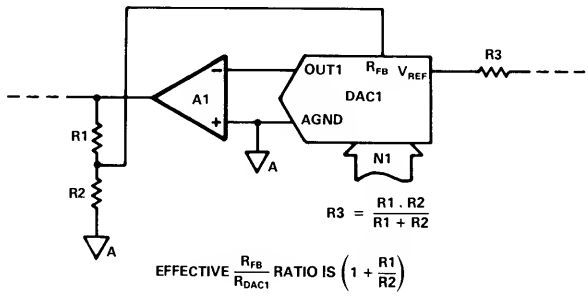


Figure 8. Recommended Way to Implement Fixed R_{FB}/R_{DAC1} Ratio

A second method of realizing a repeatable gain is to replace the feedback resistor R_{FB} in Figure 3 with a programmable feedback resistor. A second CMOS DAC placed in the feedback loop behaves as a programmable resistance and allows the circuit gain to be digitally programmed. Such a circuit is shown in Figure 9.

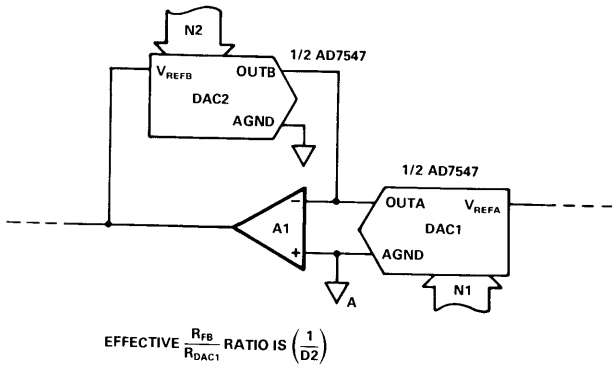


Figure 9. Recommended Way to Implement Programmable R_{FB}/R_{DAC1} Ratio

The effective feedback resistance has a value equal to

$$R_{FB} = \frac{R_{DAC2}}{D2}$$

where R_{DAC2} is the DAC ladder resistance of the feedback DAC and D2 is the fractional representation of the digital input data to the feedback DAC. The V_{RATIO} expression of Equation 5 now becomes

$$V_{RATIO} = \frac{V_{OUT}}{V_{REF}} = \frac{1}{1+D1\left(\frac{R_{DAC2}}{R_{DAC1} \cdot D2}\right)}$$

where D1 and R_{DAC1} relate to the primary DAC. If both DACs are on the same monolithic chip, then they will have identical ladder impedances. This simplifies the V_{RATIO} expression to

$$V_{RATIO} = \frac{1}{1+D1\left(\frac{1}{D2}\right)}$$

Both DACs will generally have the same resolution, n, so that the V_{RATIO} expression is shown finally to be proportional to the codes in the two DACs

$$V_{RATIO} = \frac{1}{1+N1\left(\frac{1}{N2}\right)}$$

where N1 and N2 are the codes applied to DAC1 and DAC2 respectively. Thus the R_{FB}/R_{DAC1} ratio is now solely determined by the code N2 in the feedback DAC.

To find this code, the denominators of Equation 4 and the final V_{RATIO} expression above are equated for the condition when the spindle speed is at its maximum. Using the previous example with $R_{MAX}/R_{MIN} = 2.5$, $X = 1$ and $N1 = 4095_{10}$ the correct code for DAC2 is found to be $N2 = 2730_{10}$. This code is loaded into DAC2 and is not changed thereafter. Suitable monolithic dual 12-bit DACs for this application are the AD7537/AD7547 family from Analog Devices which are available in skinny 24-pin DIP packages or in standard surface mount packages. The AD7537 with its 8+4 bit loading structure is suitable for 8-bit bus systems, while for 16-bit bus systems the AD7547, with its parallel 12-bit loading structure, is more suitable.

The programmable solution to realizing the R_{FB}/R_{DAC1} ratio raises the intriguing possibility of building a universal drive capable of reading disks of different diameters. The disks would need to have the same R_{MIN} dimension and the same maximum spindle speed f_S max. Recorded on the innermost sectors of such disks would be R_{MAX} information and the number of programmable speeds required. The drive would read this information at power-on at the standard maximum spindle speed and set the circuit parameters accordingly, a universal drive.